

FIG. 1
PRIOR ART

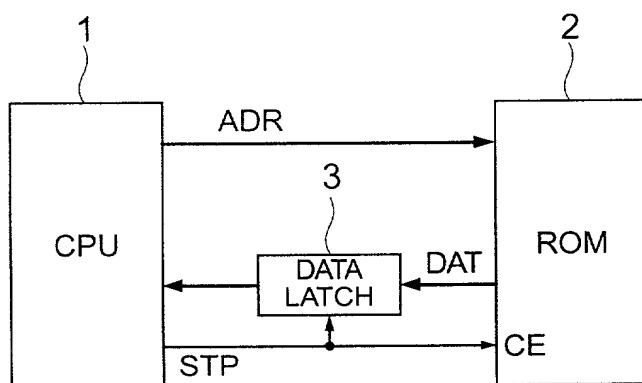
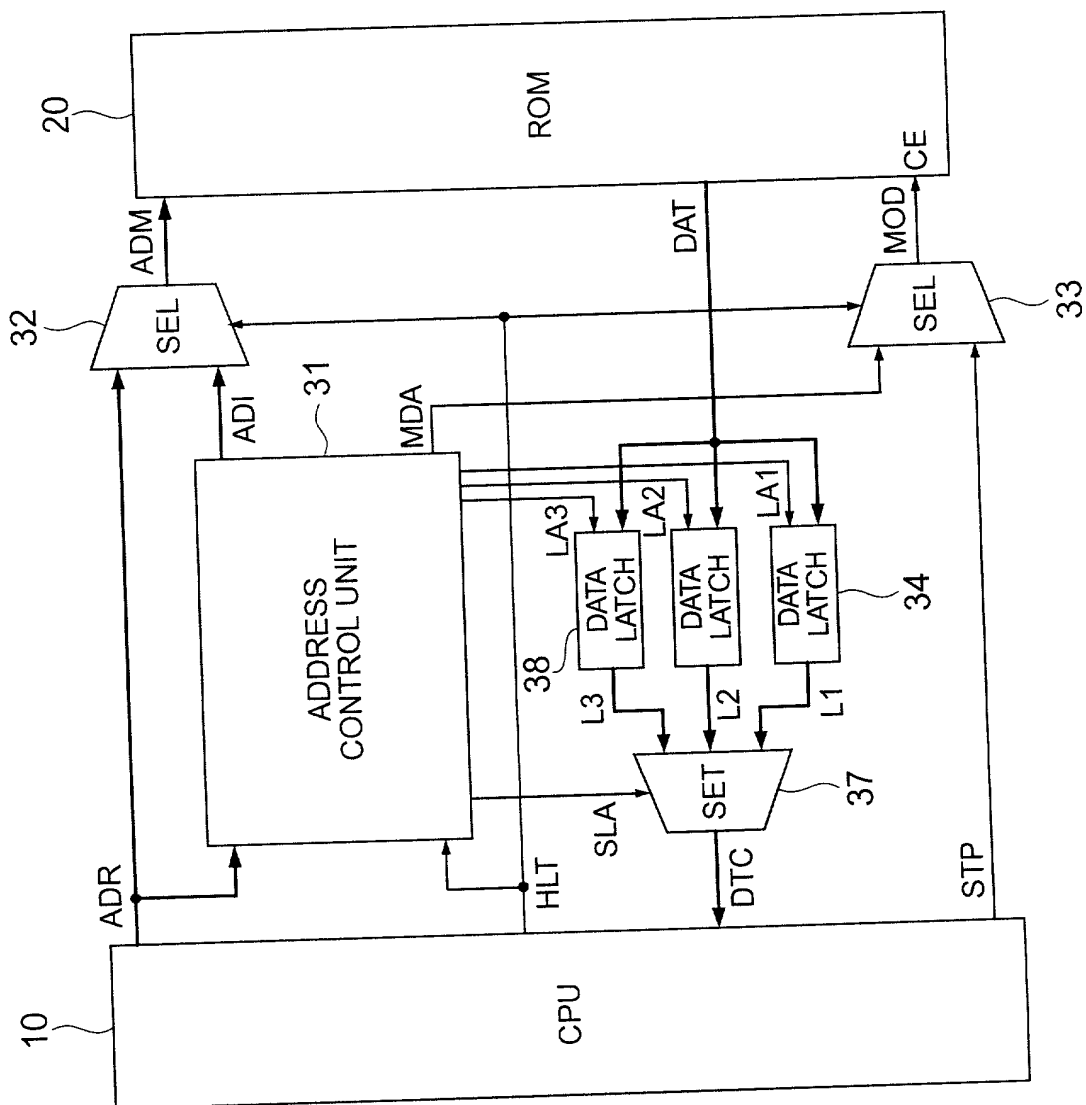


FIG. 2



The timing diagram illustrates the sequence of events for the 68000 microprocessor across eight time intervals (t1 to t8). The signals shown are:

- ADR (Address):** Consists of five 16-bit address words (AD1 to AD5). AD1 is active in t1, AD2 in t2, AD3 in t3, AD4 in t4, and AD5 in t5.
- HLT (Halt):** A control signal that transitions from Low (L) to High (H) at the start of t2 and remains High through t5.
- ADM (Address Match):** Consists of five 16-bit address match words (AD1 to AD5). AD1 is active in t1, AD2 in t2, AD3 in t3, AD4 in t4, and AD5 in t5.
- MOD (Mode):** A control signal that transitions from Low (L) to High (H) at the start of t4 and remains High through t5.
- DAT (Data):** Consists of five 16-bit data words (DT1 to DT5). DT1 is active in t1, DT2 in t2, DT3 in t3, DT4 in t4, and DT5 in t5.
- L1 (Level 1 Cache):** Consists of three 16-bit data words (L1, L2, L3). L1 is active in t1, L2 in t2, and L3 in t3.
- L2 (Level 2 Cache):** Consists of three 16-bit data words (L2, L3, L4). L2 is active in t2, L3 in t3, and L4 in t4.
- L3 (Level 3 Cache):** Consists of three 16-bit data words (L3, L4, L5). L3 is active in t3, L4 in t4, and L5 in t5.
- DTC (Data Transfer Control):** Consists of five 16-bit data transfer control words (DTC1 to DTC5). DTC1 is active in t1, DTC2 in t2, DTC3 in t3, DTC4 in t4, and DTC5 in t5.

FIG. 4

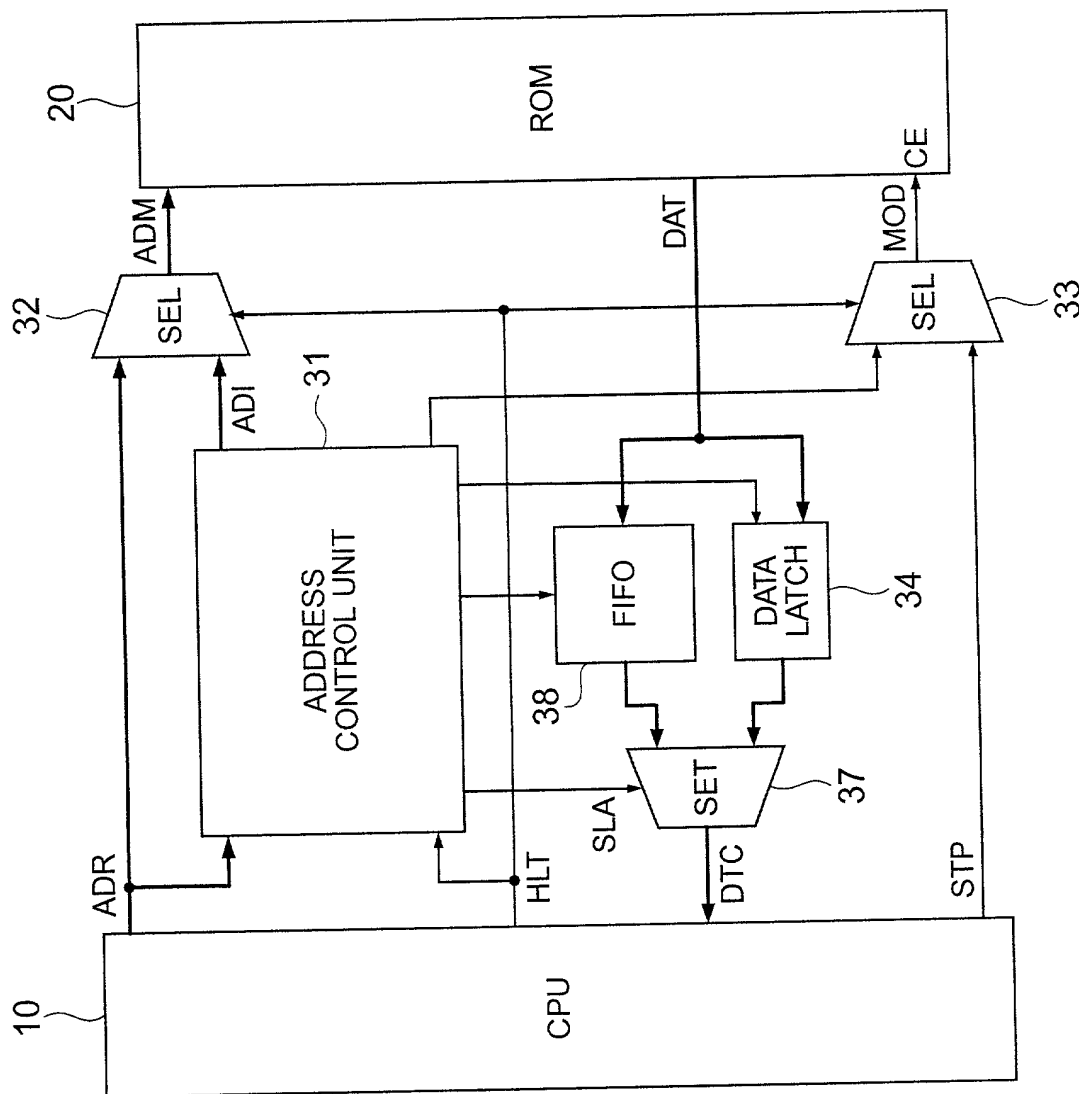


FIG. 5

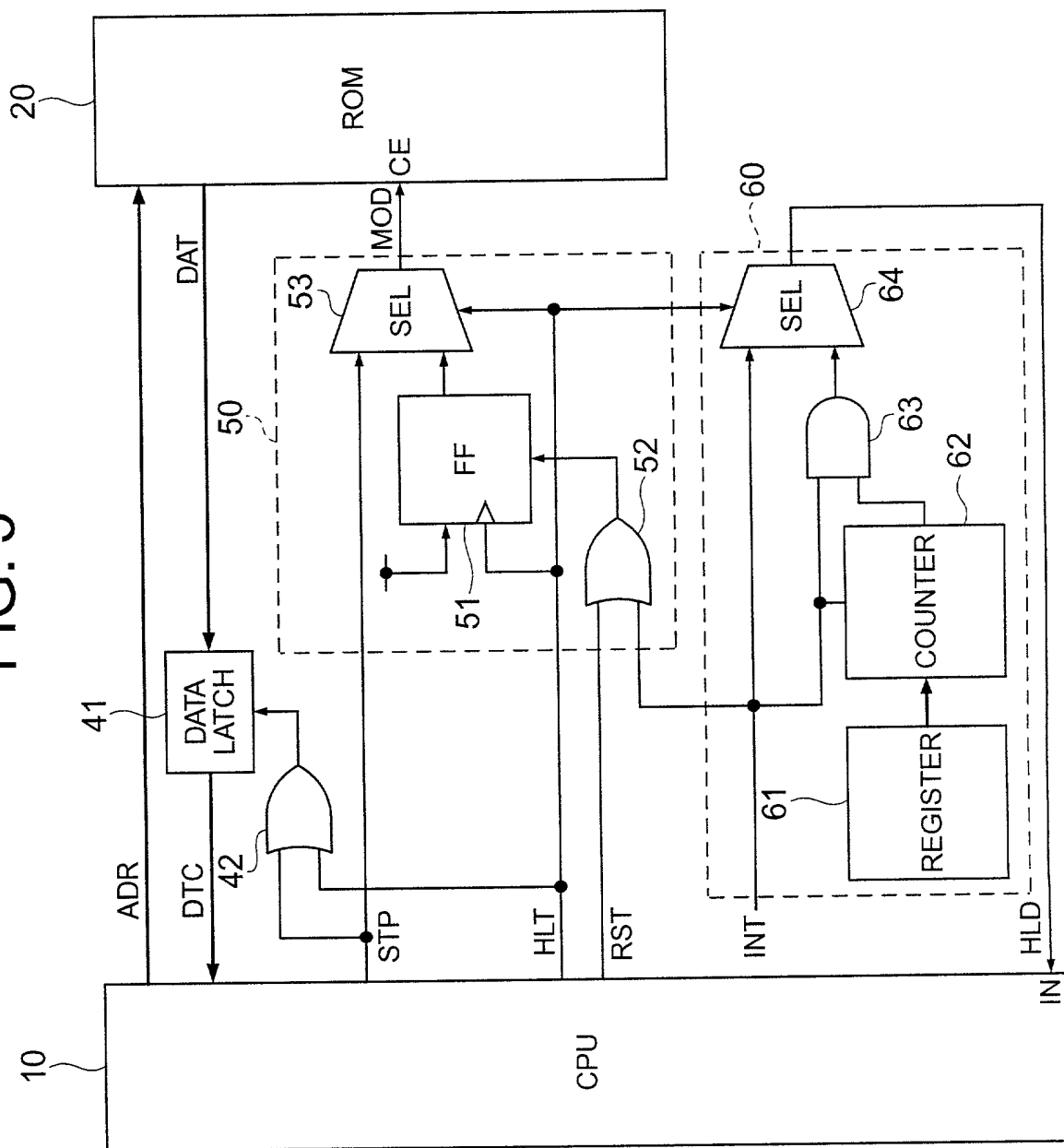


FIG. 6

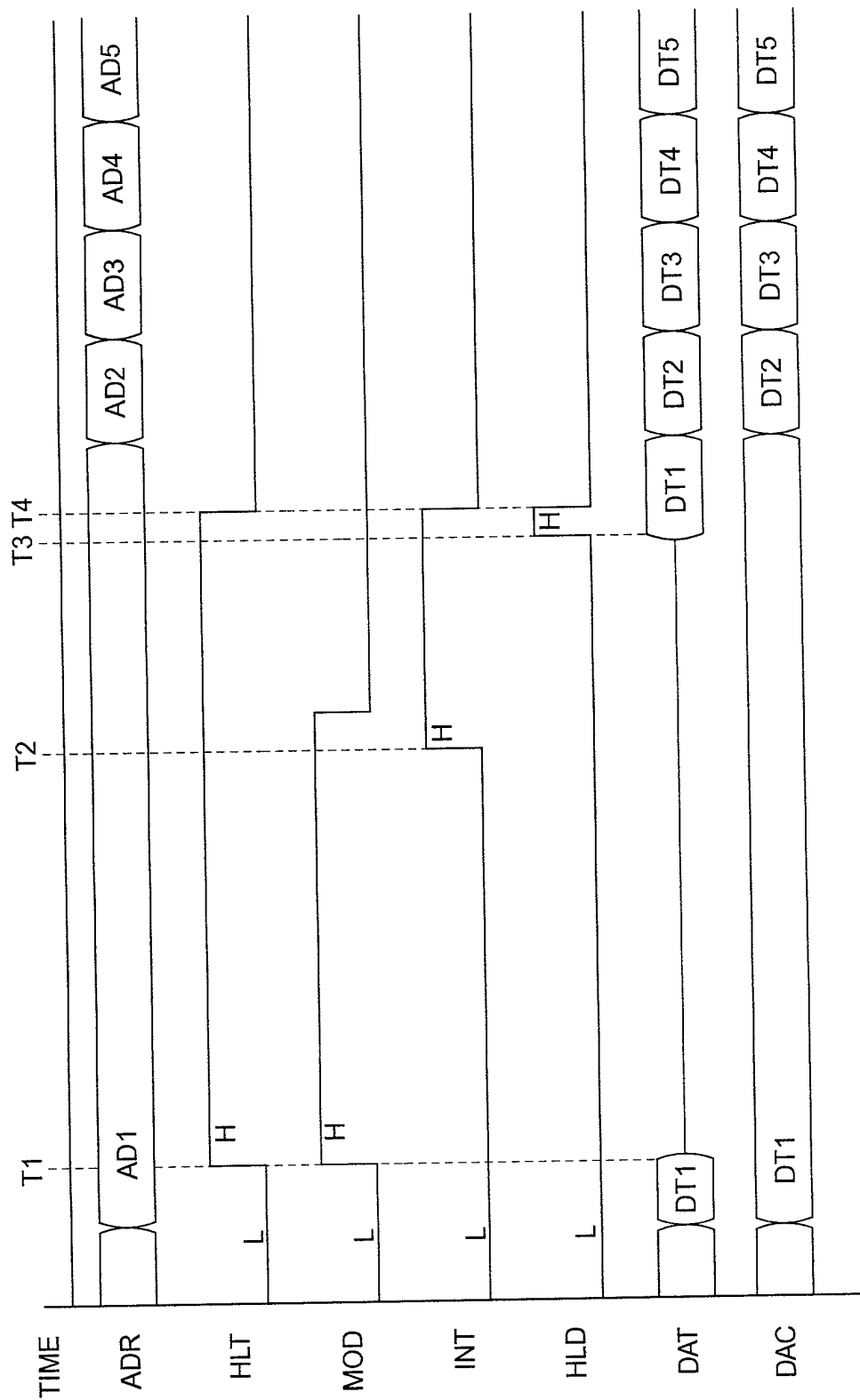


FIG. 7

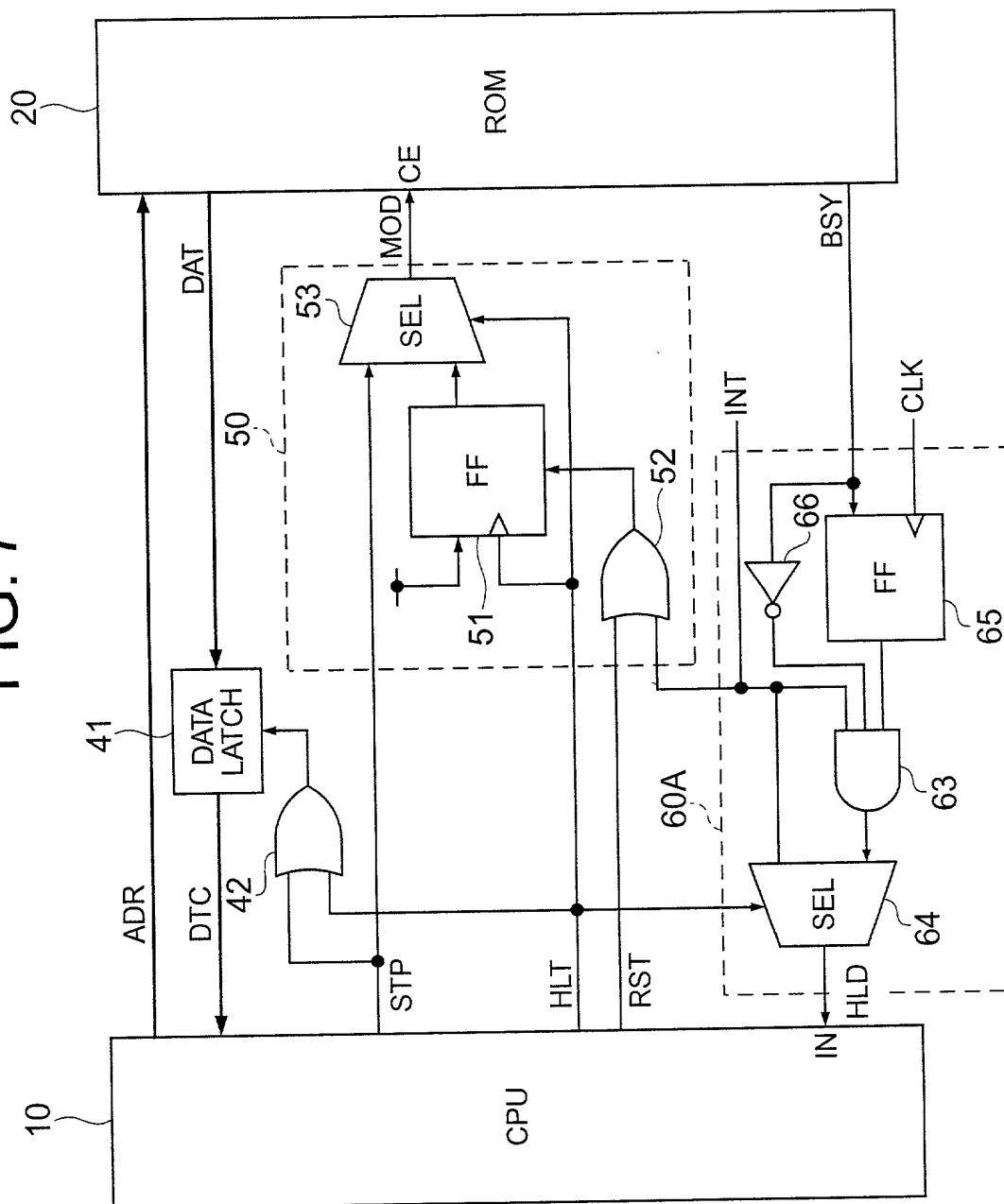


FIG. 8

